IN THE CLAIMS

Claim 1 (currently amended): A method for refreshing a memory device, comprising:

providing a memory cell having first and second memory locations;

generating a first updated latch value for a normal bit of a byte;

writing the first updated latch value to the first memory location during a clock cycle;

generating a second updated latch value for a complementary bit of a byte; and

writing the second updated latch value to the second memory location during a subsequent clock cycle.

Claim 2 (original): The method of claim 1, wherein generating the first updated latch value includes performing a logic operation on a value of the first memory location and a first data value.

Claim 3 (original): The method of claim 2, wherein generating the second updated latch value includes performing a logic operation on a value of the second memory location and a second data value.

Claim 4 (original): The method of claim 2, wherein performing the logic operation includes ORing the value of the first memory location and the first data value.

Claim 5 (original): The method of claim 4, wherein generating the second updated latch value includes performing a logic operation on a value of the second memory location and a second data value.

Claim 6 (original): The method of claim 5, wherein performing the logic operation includes ORing the value of the second memory location and the second data value.

Claim 7 (original): The method of claim 1, wherein writing the first updated latch value to the first memory location includes latching the first updated latch value in response to at least one control signal.

Claim 8 (original): The method of claim 7, wherein the at least one control signal comprises a first control signal indicative of a value of a first data value and a second control signal indicative of a status of a read operation.

Claim 9 (original): The method of claim 8, wherein writing the second updated latch value to the second memory location includes latching the second updated latch value in response to at least one control signal.

Claim 10 (original): The method of claim 9, wherein the at least one control signal comprises a first complementary control signal indicative of a value of the second data value and a second complementary control signal indicative of a status of the read operation.

Claim 11 (currently amended): A method for operating a memory device, comprising:

refreshing a normal bit of a byte stored in the memory device during a clock cycle; and

refreshing a complementary bit of the byte stored in the memory device during a different clock cycle.

Claim 12 (original): The method of claim 11, wherein refreshing the normal bit comprises:

receiving first and second control signals at a first latch of the memory device;

latching a logic value of the normal bit at a first node in response to the first and second control signals;

generating a first update value by performing a logic function on the logic value and a first data value; and

transmitting the first update value of the normal bit to an output terminal of the first latch in response to a third control signal.

Claim 13 (original): The method of claim 12, further including transmitting the first update value of the normal bit to an output terminal of a second latch in response to a fourth control signal.

Claim 14 (original): The method of claim 13, wherein refreshing the complementary bit comprises:

receiving the first and fifth control signals at a second latch of the memory device;

latching a second update value of the complementary bit at a second node in response to the first and fifth control signals; and

transmitting the second update value of the complementary bit to an output terminal of the second latch in response to a sixth control signal.

Claim 15 (original): A method for refreshing a memory device, comprising:

providing the memory device having a data latch, a complementary data latch, and a write latch;

applying first and second control signals to the data latch, wherein the first control signal represents a programming status of a memory location;

latching a memory value in the data latch in response to the first and second control signals;

performing a logic operation on the memory value and a data value to generate a refresh value;

transmitting the refresh value to an output terminal of the write latch;

applying the first control signal and a third control signal to the complementary data latch;

latching a complementary refresh value in the complementary data latch in response to the first control signal and a third control signal; and

transmitting the complementary refresh value to the output terminal of the write latch.

Claim 16 (original): The method of claim 15, wherein performing the logic operation on the memory value and the data value includes ORing the memory value and the data value to generate the refresh value.

Claim 17 (original): The method of claim 16, further including transmitting the refresh value at the first node of the data latch to an output terminal of the data latch in response to a fourth control signal.

Claim 18 (original): The method of claim 17, further including transmitting the logic low level at the first node of the data latch to an output terminal of the write latch in response to a fifth control signal.

Claim 19 (original): The method of claim 18, wherein applying the first and third control signals produces a logic low level at a first node of the complementary data latch.

Claim 20 (original): The method of claim 19, further including transmitting the logic low level at the first node of the complementary data latch to the output terminal of the data latch in response to the fourth control signal.

Claim 21 (original): The method of claim 20, further including transmitting the logic low level at the first node of the complementary data latch to the output terminal of the write latch in response to the fifth control signal.

Claim 22 (original): The method of claim 21, wherein the logic low level at the first node of the data latch is produced during the first half of a first clock cycle, the logic low level at the first node of the data latch is transmitted to the output terminal of the write latch during a second half of the first clock cycle, the logic low level at the first node of the complementary data latch is produced during the first half of a second clock cycle, and the logic low level at the first node of the complementary data latch is transmitted to the output terminal of the write latch during a second half of the second clock cycle.

Claims 23-32 (canceled)

Claim 33 (new): The method of claim 11, wherein the different clock cycle is a subsequent clock cycle.

Claim 34 (new): The method of claim 11, wherein the clock cycle is a subsequent clock cycle.